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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,660	07/27/2004	I-Shu Lee	13015-US-PA	4659
31561	7590	09/26/2008		
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			EXAMINER	
			XIAO, KE	
			ART UNIT	PAPER NUMBER
			2629	
			NOTIFICATION DATE	DELIVERY MODE
			09/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW
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Office Action Summary	Application No.	Applicant(s)	
	10/710,660	LEE, I-SHU	
Examiner	Art Unit		
Ke Xiao	2629		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 July 2008.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1 and 3-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1 and 3-9 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 2002/0105279).

Regarding **Claim 1**, Kimura teaches an active matrix organic light emitting diode (AMOLED) driving control circuit for dynamically adjusting the white balance of an AMOLED display panel (Kimura, Fig. 1), comprising:

a gate driving circuit for generating a horizontal scan signal to control a scan line of the AMOLED display panel (Kimura, Fig. 1 element 104);

a source driving circuit for applying a video data to the AMOLED display panel according to the horizontal scan signal (Kimura, Fig. 1 element 103);

a programmable voltage generator for generating a plurality of programmable voltage sources that serves as power sources for driving red, green and blue pixels within the AMOLED display panel (Kimura, Figs. 1, 6, 7 and 19, RGB voltages element 106 and 108); and

a timing control circuit coupled to the gate driving circuit, the source driving circuit and the programmable voltage generator (Kimura, Figs. 6, 16A and 16B Video, CLK and SP signals) comprising:

a source and gate timing data control circuit for controlling the timing of the submission for the video data between the gate driving circuit and the source driving circuit (Kimura, Figs. 6, 16A and 16B Video, CLK and SP signals);

an interface processing circuit serving as a signal transmission interface (Kimura, Fig. 6 video circuit including CLK); and

a white balance adjusting circuit coupled to the source and gate timing data control circuit and the interface processing circuit for adjusting the parameters for setting the voltage value of the programmable voltage sources according to the display time and an average luminance value having a value higher than a fixed value of the AMOLED display panel and submitting the parameters to the programmable voltage generator through the interface processing circuit (Kimura, Figs. 1 and 6 video circuit including CLK),

Kimura fails to teach the number of pixels having a displayed gray level higher than a fixed value. As detailed above Kimura teaches comparing a threshold value to an *average* error value in order to determine white balance, whereas the applicant uses a threshold value of a *number of errors*. Since the applicant has not disclosed that counting the number of errors instead of using an average error value has a special purpose, solves a specific problem or provides a distinct advantage, examiner believes

that it would have been an obvious matter of design choice to one of ordinary skill in the art at the time of the invention to replace the average error threshold of Kimura with the number error threshold because either one would perform white balance equally as well.

Kimura further fails to teach wherein the source an gate timing data control circuit, the interface processing circuit and the white balance adjusting circuit are manufactured on a single chip or integrated circuit to form the timing control circuit.

The examiner takes official notice that it is well known in the art to combine or modulate circuitry of any kind into a single integrated circuit or a plurality of integrated circuits. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine all the circuits of Kimura into a single integrated circuit in order to reduce production costs and manufacturing difficulties.

Regarding **Claims 3 and 9**, Kimura teaches wherein the white balance adjusting circuit at least (Kimura, Fig. 6) comprises:

a first counter for counting the number of data values the adjusting circuit is sampling over a preset period of time (Kimura, Fig. 6 element 123);

a sampler for obtaining the sum of the sampled data values (Kimura, Fig. 6 element 129);

a division circuit to divide the sum by the number of data values sampled in order to obtain an average data value (Kimura, Fig. 6 element 124);

a comparator for comparing the average data value to a reference data value (Kimura, Fig. 6 element 121);

and if the error is greater than a reference error value using a parameter setting unit, coupled to the comparator, to provide the parameter for setting the voltage value of the programmable voltage sources according to the adjusting signal and transmitting the parameter to the programmable voltage generator through the interface processing circuit (Kimura, Fig. 6 element 127, 128 and 122 and 106).

Kimura fails to teach the combination of a first comparator, a counter, a second comparator, and an AND logic unit as claimed when determining how to adjust the programmable voltage source. As detailed above Kimura teaches using threshold value of an average error value in order to determine white balance whereas the applicant uses a threshold value of a *number of errors*. Since the applicant has not disclosed that counting the number of errors instead of using an average error value has a special purpose, solves a specific problem or provides a distinct advantage, examiner believes that it would have been an obvious matter of design choice to one of ordinary skill in the art at the time of the invention to replace the average error threshold of Kimura with the number error threshold because either one would perform white balance equally as well.

Regarding **Claims 4, 5 and 6**, Kimura fails to teach PROM, EEPROM or flash Memory for storing preset data, preset count and preset time periods. Instead Kimura teaches storing preset values in registers (Kimura, Fig. 6, 125 and 127). The examiner

takes official notice that it is well known in the art that flash memory, which also qualifies as PROM and EEPROM, is used as registers. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the generic registers of Kimura with flash memory in order to provide a reliable, nonvolatile form of storage.

Regarding **Claim 7**, Kimura further teaches wherein the interface processing circuit comprises a serial transmission interface (Kimura, Figs. 1, 6 and 16 video signals CLK and SP signals are all transferred serially from frame to frame).

Regarding **Claim 8**, Kimura teaches a method of dynamically adjusting the white balance of an AMOLED display panel using an AMOLED driving control circuit (Kimura, Fig. 1) comprising:

providing a plurality of programmable voltage sources to serve as power sources for driving red, green and blue pixels within the AMOLED display panel (Kimura, Figs. 1, 6 and 19); and

adjusting the voltage value of the programmable voltage sources dynamically according to the display time and if an average luminance of the pixels measured of the AMOLED display panel is higher than a fixed value (Kimura, Fig. 6).

Kimura fails to teach the number of pixels having a displayed gray level higher than a fixed value. As detailed above Kimura teaches comparing a threshold value to an *average* error value in order to determine white balance, whereas the applicant uses a threshold value of a *number of errors*. Since the applicant has not disclosed that

counting the number of errors instead of using an average error value has a special purpose, solves a specific problem or provides a distinct advantage, examiner believes that it would have been an obvious matter of design choice to one of ordinary skill in the art at the time of the invention to replace the average error threshold of Kimura with the number error threshold because either one would perform white balance equally as well.

Response to Arguments

Applicant's arguments filed July 3rd 2008 have been fully considered but they are not persuasive.

Regarding Claim 1, the applicant argues that the timing control circuit as claimed is not inherent to the display device of Kimura. The examiner respectfully disagrees. Kimura clearly teaches that the timing control circuit is connected to the gate driver the source driver and the programmable voltage driver, and it *must* inherently be supplying all three with timing signals and control signals in order to allow all of them to operate synchronously; therefore the control circuit is indirectly making the adjustments to the programmable voltage driver as claimed.

Applicant's arguments with respect to the newly added limitations of claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629